

*Advance Information*

MCF5307PB/D  
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MCF5307 Integrated  
Microprocessor Product Brief



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This document provides an overview of the MCF5307 ColdFire processor. It includes general descriptions of the modules and features incorporated in the MCF5307.

## 1.1 Features

The MCF5307 integrated microprocessor combines a V3 ColdFire processor core with the following components, as shown in Figure 1:

- 8-Kbyte unified cache
- 4-Kbyte on-chip SRAM
- Integer/fractional multiply-accumulate (MAC) unit
- Divide unit
- System debug interface
- DRAM controller for synchronous and asynchronous DRAM
- Four-channel DMA controller
- Two general-purpose timers
- Two UARTs
- I<sup>2</sup>C™ interface
- Parallel I/O interface
- System integration module (SIM)

Designed for embedded control applications, the MCF5307 delivers 75 Dhrystone 2.1 MIPS at 90 MHz while minimizing system costs.

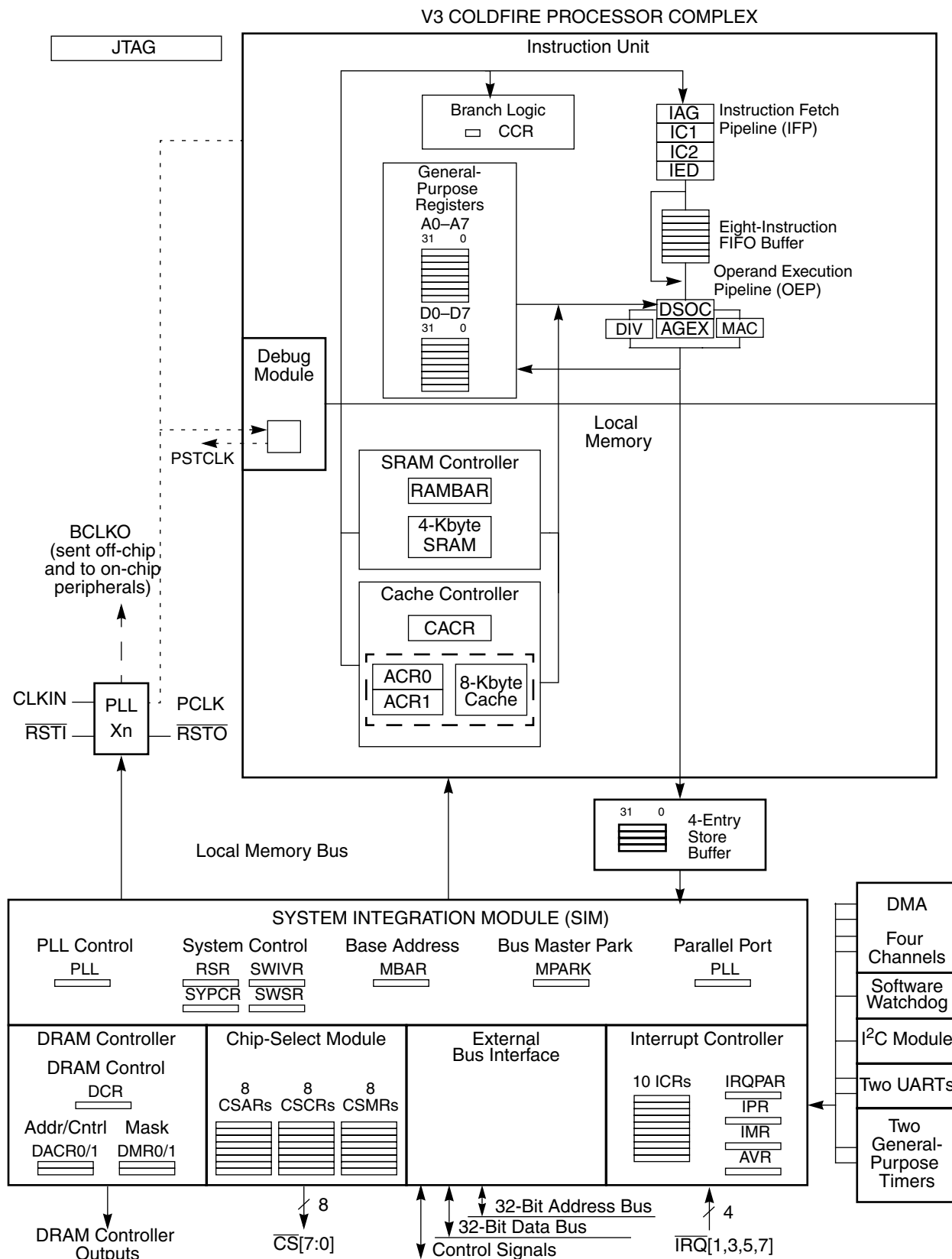


Figure 1. MCF5307 Block Diagram

Features common to many embedded applications, such as DMAs, various DRAM controller interfaces, and on-chip memories, are integrated using advanced process technologies.

The MCF5307 extends the legacy of Motorola's 68K family by providing a compatible path for 68K and ColdFire customers in which development tools and customer code can be leveraged. In fact, customers moving from 68K to ColdFire can use code translation and emulation tools that facilitate modifying 68K assembly code to the ColdFire architecture.

Based on the concept of variable-length RISC technology, the ColdFire family combines the architectural simplicity of conventional 32-bit RISC with a memory-saving, variable-length instruction set. In defining the ColdFire architecture for embedded processing applications, a 68K-code compatible core combines performance advantages of a RISC architecture with the optimum code density of a streamlined, variable-length M68000 instruction set.

By using a variable-length instruction set architecture, embedded system designers using ColdFire RISC processors enjoy significant advantages over conventional fixed-length RISC architectures. The denser binary code for ColdFire processors consumes less memory than many fixed-length instruction set RISC processors available. This improved code density means more efficient system memory use for a given application and allows use of slower, less costly memory to help achieve a target performance level.

The MCF5307 is the first standard product to implement the Version 3 ColdFire microprocessor core. To reach higher levels of frequency and performance, numerous enhancements were made to the V2 architecture. Most notable are a deeper instruction pipeline, branch acceleration, and a unified cache, which together provide 75 (Dhrystone 2.1) MIPS at 90 MHz. Increasing the internal speed of the core also allows higher performance while providing the system designer with an easy-to-use lower speed system interface. The processor complex frequency is an integer multiple, 2 to 4 times, of the external bus frequency. The core clock can be stopped to support a low-power mode.

Serial communication channels are provided by an I<sup>2</sup>C interface module and two programmable full-duplex UARTs. Four channels of DMA allow for fast data transfer using a programmable burst mode independent of processor execution. The two 16-bit general-purpose multimode timers provide separate input and output signals. For system protection, the processor includes a programmable 16-bit software watchdog timer. In addition, common system functions such as chip selects, interrupt control, bus arbitration, and an IEEE 1149.1 JTAG module are included. A sophisticated debug interface supports background-debug mode plus real-time trace and debug with expanded flexibility of on-chip breakpoint registers. This interface is present in all ColdFire standard products and allows common emulator support across the entire family of microprocessors.

## 1.2 MCF5307 Features

The following list summarizes MCF5307 features:

- ColdFire processor core
  - Variable-length RISC, clock-multiplied Version 3 microprocessor core
  - Fully code compatible with Version 2 processors
  - Two independent decoupled pipelines: four-stage instruction fetch pipeline (IFP) and two-stage operand execution pipeline (OEP)
  - Eight-instruction FIFO buffer provides decoupling between the pipelines
  - Branch prediction mechanisms for accelerating program execution
  - 32-bit internal address bus supporting 4 Gbytes of linear address space

- 32-bit data bus
- 16 user-accessible, 32-bit-wide, general-purpose registers
- Supervisor/user modes for system protection
- Vector base register to relocate exception-vector table
- Optimized for high-level language constructs
- Multiply and accumulate unit (MAC)
  - High-speed, complex arithmetic processing for DSP applications
  - Tightly coupled to the OEP
  - Three-stage execute pipeline with one clock issue rate for 16 x 16 operations
  - 16 x 16 and 32 x 32 multiplies support, all with 32-bit accumulate
  - Signed or unsigned integer support, plus signed fractional operands
- Hardware integer divide unit
  - Unsigned and signed integer divide support
  - Tightly coupled to the OEP
  - 32/16 and 32/32 operation support producing quotient and/or remainder results
- 8-Kbyte unified cache
  - Four-way set-associative organization
  - Operates at higher processor core frequency
  - Provides pipelined, single-cycle access to critical code and data
  - Supports write-through and copyback modes
  - Four-entry, 32-bit store buffer to improve performance of operand writes
- 4-Kbyte SRAM
  - Programmable location anywhere within 4-Gbyte linear address space
  - Higher core-frequency operation
  - Pipelined, single-cycle access to critical code or data
- DMA controller
  - Four fully programmable channels: two support external requests
  - Dual-address and single-address transfer support with 8-, 16-, and 32-bit data capability
  - Source/destination address pointers that can increment or remain constant
  - 24-bit transfer counter per channel
  - Operand packing and unpacking supported
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle steal support
  - Two-bus-clock internal access
  - Automatic DMA transfers from on-chip UARTs using internal interrupts
- DRAM controller
  - Synchronous DRAM (SDRAM), extended-data-out (EDO) DRAM, and fast page mode support

- Up to 512 Mbytes of DRAM
- Programmable timer provides CAS-before-RAS refresh for asynchronous DRAMs
- Support for two separate memory blocks
- Two UARTs
  - Full-duplex operation
  - Programmable clock
  - Modem control signals available ( $\overline{\text{CTS}}$ ,  $\overline{\text{RTS}}$ )
  - Processor-interrupt capability
- Dual 16-bit general-purpose multiple-mode timers
  - 8-bit prescaler
  - Timer input and output pins
  - Processor-interrupt capability
  - Up to 22-nS resolution at 45 MHz
- I<sup>2</sup>C module
  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
  - Fully compatible with industry-standard I<sup>2</sup>C bus
  - Master or slave modes support multiple masters
  - Automatic interrupt generation with programmable level
- System interface module (SIM)
  - Chip selects provide direct interface to 8-, 16-, and 32-bit SRAM, ROM, FLASH, and memory-mapped I/O devices
  - Eight fully programmable chip selects, each with a base address register
  - Programmable wait states and port sizes per chip select
  - User-programmable processor clock/input clock frequency ratio
  - Programmable interrupt controller
  - Low interrupt latency
  - Four external interrupt request inputs
  - Programmable autovector generator
  - Software watchdog timer
- 16-bit general-purpose I/O interface
- IEEE 1149.1 test (JTAG) module
- System debug support
  - Real-time trace for determining dynamic execution path while in emulator mode
  - Background debug mode (BDM) for debug features while halted
  - Real-time debug support, including 6 user-visible hardware breakpoint registers supporting a variety of breakpoint configurations
  - Supports comprehensive emulator functions through trace and breakpoint logic

**ColdFire Module Description**

- On-chip PLL
  - Supports processor clock/bus clock ratios of 66/33, 66/22, 66/16.5, 90/45, 90/30, and 90/22.5
  - Supports low-power mode
- Product offerings
  - 75 Dhrystone 2.1 MIPS at 90 MHz
  - Implemented in 0.35  $\mu$ , triple-layer-metal process technology with 3.3-V operation (5.0-V compliant I/O pads)
  - 208-pin plastic QFP package
  - 0°–70° C operating temperature

## 1.2.1 Process

The MCF5307 is manufactured in a 0.35- $\mu$  CMOS process with triple-layer-metal routing technology. This process combines the high performance and low power needed for embedded system applications. Inputs are 3.3-V tolerant; outputs are CMOS or open-drain CMOS with outputs operating from VDD + 0.5 V to GND - 0.5 V, with guaranteed TTL-level specifications.

## 1.3 ColdFire Module Description

The following sections provide overviews of the various modules incorporated in the MCF5307.

### 1.3.1 ColdFire Core

The Version 4 ColdFire core consists of two independent and decoupled pipelines to maximize performance—the instruction fetch pipeline (IFP) and the operand execution pipeline (OEP).

#### 1.3.1.1 Instruction Fetch Pipeline (IFP)

The four-stage instruction fetch pipeline (IFP) is designed to prefetch instructions for the operand execution pipeline (OEP). Because the fetch and execution pipelines are decoupled by a eight-instruction FIFO buffer, the fetch mechanism can prefetch instructions in advance of their use by the OEP, thereby minimizing the time stalled waiting for instructions. To maximize the performance of branch instructions, the Version 3 IFP implements a branch prediction mechanism. Backward branches are predicted to be taken. The prediction for forward branches is controlled by a bit in the Condition Code Register (CCR). These predictions allow the IFP to redirect the fetch stream down the path predicted to be taken well in advance of the actual instruction execution. The result is significantly improved performance.

#### 1.3.1.2 Operand Execution Pipeline (OEP)

The prefetched instruction stream is gated from the FIFO buffer into the two-stage OEP. The OEP consists of a traditional two-stage RISC compute engine with a register file access feeding an arithmetic/logic unit (ALU). The OEP decodes the instruction, fetches the required operands and then executes the required function.

### 1.3.1.3 MAC Module

The MAC unit provides signal processing capabilities for the MCF5307 in a variety of applications including digital audio and servo control. Integrated as an execution unit in the processor's OEP, the MAC unit implements a three-stage arithmetic pipeline optimized for 16 x 16 multiplies. Both 16- and 32-bit input operands are supported by this design in addition to a full set of extensions for signed and unsigned integers, plus signed, fixed-point fractional input operands.

### 1.3.1.4 Integer Divide Module

Integrated into the OEP, the divide module performs operations using signed and unsigned integers. The module supports word and longword divides producing quotients and/or remainders.

### 1.3.1.5 8-Kbyte Unified Cache

The MCF5307 architecture includes an 8-Kbyte unified cache. This four-way, set-associative cache provides pipelined, single-cycle access on cached instructions and operands.

As with all ColdFire caches, the cache controller implements a non-lockup, streaming design. The use of processor-local memories decouples performance from external memory speeds and increases available bandwidth for external devices or the on-chip 4-channel DMA.

The cache implements line-fill buffers to optimize 16-byte line burst accesses. Additionally, the cache supports copyback, write-through, or cache-inhibited modes. A 4-entry, 32-bit buffer is used for cache line push operations and can be configured for deferred write buffering in write-through or cache-inhibited modes.

### 1.3.1.6 Internal 4-Kbyte SRAM

The 4-Kbyte on-chip SRAM module provides pipelined, single-cycle access to memory regions mapped to these devices. The memory can be mapped to any 0-modulo-32K location in the 4-Gbyte address space. The SRAM module is useful for storing time-critical functions, the system stack, or heavily-referenced data operands.

## 1.3.2 DRAM Controller

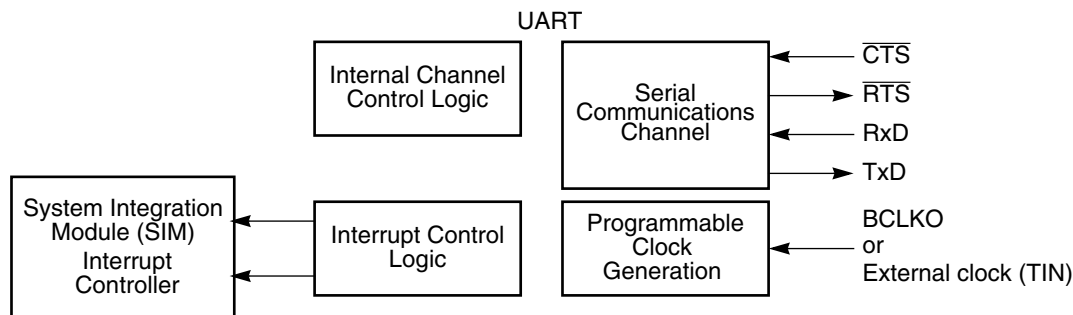
The MCF5307 DRAM controller provides a direct interface for up to two blocks of DRAM. The controller supports 8-, 16-, or 32-bit memory widths and can easily interface to PC-100 DIMMs. A unique addressing scheme allows for increases in system memory size without rerouting address lines and rewiring boards. The controller operates in normal mode or in page mode and supports SDRAMs and EDO DRAMs.

## 1.3.3 DMA Controller

The MCF5307 provides four fully programmable DMA channels for quick data transfer. Dual- and single-address modes support bursting and cycle steal. Data transfers are 32 bits long with packing and unpacking supported along with an auto-alignment option for efficient block transfers. Automatic block transfers from on-chip serial UARTs are also supported through the DMA channels.

### 1.3.4 UART Modules

The MCF5307 contains two UARTs, which function independently. Either UART can be clocked by the system bus clock, eliminating the need for an external crystal. Each UART module interfaces directly to the CPU, as shown in Figure 2.



**Figure 2. UART Module Block Diagram**

Each UART module consists of the following major functional areas:

- Serial communication channel
- 16-bit divider for clock generation
- Internal channel control logic
- Interrupt control logic

Each UART contains an programmable clock-rate generator. Data formats can be 5, 6, 7, or 8 bits with even, odd, or no parity, and up to 2 stop bits in 1/16 increments. The UARTs include 4-byte and 2-byte FIFO buffers. The UART modules also provide several error-detection and maskable-interrupt capabilities. Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines.

BCLKO provides the time base through a programmable prescaler. The UART time scale can also be sourced from a timer input. Full-duplex, auto-echo loopback, local loopback, and remote loopback modes allow testing of UART connections. The programmable UARTs can interrupt the CPU on various normal or error-condition events.

### 1.3.5 Timer Module

The timer module includes two general-purpose timers, each of which contains a free-running 16-bit timer for use in any of three modes. One mode captures the timer value with an external event. Another mode triggers an external signal or interrupts the CPU when the timer reaches a set value, while a third mode counts external events.

The timer unit has an 8-bit prescaler that allows programming of the clock input frequency, which is derived from the system bus cycle or an external clock input pin (TIN). The programmable timer-output pin generates either an active-low pulse or toggles the output.

### 1.3.6 I<sup>2</sup>C Module

The I<sup>2</sup>C interface is a two-wire, bidirectional serial bus used for quick data exchanges between devices. The I<sup>2</sup>C minimizes the interconnection between devices in the end system and is best suited for applications that



need occasional bursts of rapid communication over short distances among several devices. The I<sup>2</sup>C can operate in master, slave, or multiple-master modes.

## 1.3.7 System Interface

The MCF5307 processor provides a direct interface to 8-, 16-, and 32-bit FLASH, SRAM, ROM, and peripheral devices through the use of fully programmable chip selects and write enables. Support for burst ROMs is also included. Through the on-chip PLL, users can input a slower clock (16.6 to 45 MHz) that is internally multiplied to create the faster processor clock (33.3 to 90 MHz).

### 1.3.7.1 External Bus Interface

The bus interface controller transfers information between the ColdFire core or DMA and memory, peripherals, or other devices on the external bus. The external bus interface provides up to 32 bits of address bus space, a 32-bit data bus, and all associated control signals. This interface implements an extended synchronous protocol that supports bursting operations.

Simple two-wire request/acknowledge bus arbitration between the MCF5307 processor and another bus master, such as an external DMA device, is glueless with arbitration logic internal to the MCF5307 processor. Multiple-master arbitration is also available with some simple external arbitration logic.

### 1.3.7.2 Chip Selects

Eight fully programmable chip select outputs support the use of external memory and peripheral circuits with user-defined wait-state insertion. These signals interface to 8-, 16-, or 32-bit ports. The base address, access permissions, and internal bus transfer terminations are programmable with configuration registers for each chip select.  $\overline{CS0}$  also provides global chip select functionality of boot ROM upon reset for initializing the MCF5307.

### 1.3.7.3 16-Bit Parallel Port Interface

A 16-bit general-purpose programmable parallel port serves as either an input or an output on a pin-by-pin basis.

### 1.3.7.4 Interrupt Controller

The interrupt controller provides user-programmable control of ten internal peripheral interrupts and implements four external fixed interrupt-request pins. Each internal interrupt can be programmed to any one of seven interrupt levels and four priority levels within each of these levels. Additionally, the external interrupt request pins can be mapped to levels 1, 3, 5, and 7 or levels 2, 4, 6, and 7. Autovector capability is available for both internal and external interrupts.

### 1.3.7.5 JTAG

To help with system diagnostics and manufacturing testing, the MCF5307 processor includes dedicated user-accessible test logic that complies with the IEEE 1149.1a standard for boundary-scan testability, often referred to as the Joint Test Action Group, or JTAG. For more information, refer to the IEEE 1149.1a standard.

## 1.3.8 System Debug Interface

The ColdFire processor core debug interface is provided to support system debugging in conjunction with low-cost debug and emulator development tools. Through a standard debug interface, users can access real-time trace and debug information. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators. The debug unit in the MCF5307 is a compatible upgrade to the MCF52xx debug module with added flexibility in the breakpoint registers and a new command to view the program counter (PC).

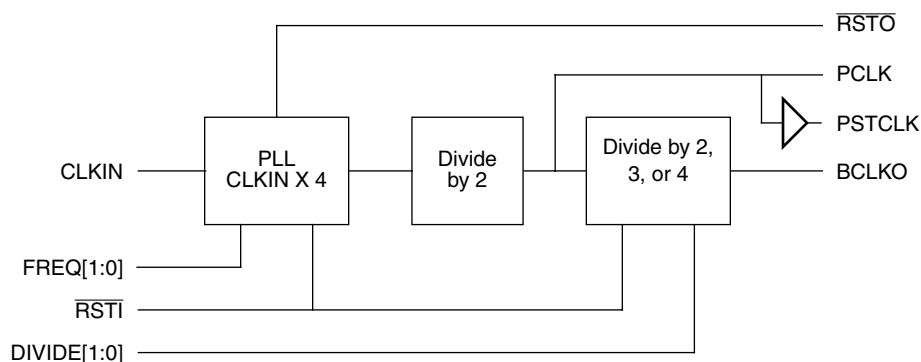
The on-chip breakpoint resources include a total of 6 programmable registers—a set of address registers (with two 32-bit registers), a set of data registers (with a 32-bit data register plus a 32-bit data mask register), and one 32-bit PC register plus a 32-bit PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception.

The MCF5307's new interrupt servicing options during emulator mode allow real-time critical interrupt service routines to be serviced while processing a debug interrupt event, thereby ensuring that the system continues to operate even during debugging.

To support program trace, the Version 3 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate.

## 1.3.9 PLL Module

The MCF5307 PLL module is shown in Figure 3.



**Figure 3. PLL Module**

The PLL module's three modes of operation are described as follows.

- Reset mode—When  $\overline{RSTI}$  is asserted, the PLL enters reset mode. At reset, the PLL asserts  $\overline{RSTO}$  from the MCF5307. The core:bus frequency ratio and other MCF5307 configuration information are sampled during reset.
- Normal mode—In normal mode, the input frequency programmed at reset is clock-multiplied to provide the processor clock (PCLK).

- Reduced-power mode—In reduced-power mode, the PCLK is disabled by executing a sequence that includes programming a control bit in the system configuration register (SCR) and then executing the STOP instruction. Register contents are retained in reduced-power mode, so the system can be reenabled quickly when an unmasked interrupt or reset is detected.

## 1.4 Programming Model, Addressing Modes, and Instruction Set

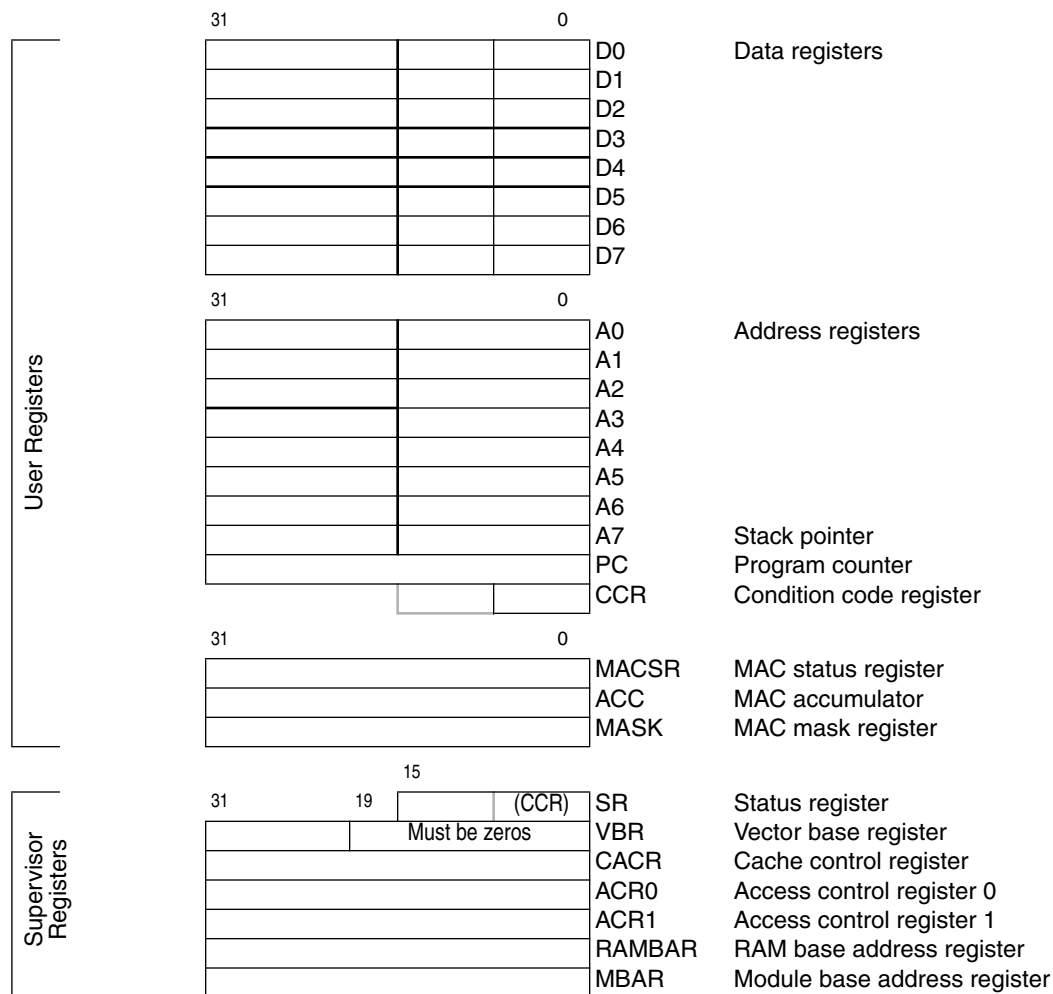
The ColdFire programming model has two privilege levels—supervisor and user. The S bit in the status register (SR) indicates the privilege level. The processor identifies a logical address that differentiates between supervisor and user modes by accessing either the supervisor or user address space.

- User mode—When the processor is in user mode ( $SR[S] = 0$ ), only a subset of registers can be accessed, and privileged instructions cannot be executed. Typically, most application processing occurs in user mode. User mode is usually entered by executing a return from exception instruction (RTE, assuming the value of  $SR[S]$  saved on the stack is 0) or a MOVE, SR instruction (assuming  $SR[S]$  is 0).
- Supervisor mode—This mode protects system resources from uncontrolled access by users. In supervisor mode, complete access is provided to all registers and the entire ColdFire instruction set. Typically, system programmers use the supervisor programming model to implement operating system functions and provide I/O control. The supervisor programming model provides access to the same registers as the user model, plus additional registers for configuring on-chip system resources, as described in Section 1.4.3, “Supervisor Registers.”

Exceptions (including interrupts) are handled in supervisor mode.

### 1.4.1 Programming Model

Figure 4 shows the MCF5307 programming model.



**Figure 4. ColdFire MCF5307 Programming Model**

## 1.4.2 User Registers

The user programming model is shown in Figure 4 and summarized in Table 1.

**Table 1. User-Level Registers**

Register	Description
Data registers (D0–D7)	These 32-bit registers are for bit, byte, word, and longword operands. They can also be used as index registers.
Address registers (A0–A7)	These 32-bit registers serve as software stack pointers, index registers, or base address registers. The base address registers can be used for word and longword operations. A7 functions as a hardware stack pointer during stacking for subroutine calls and exception handling.
Program counter (PC)	Contains the address of the instruction currently being executed by the MCF5307 processor

**Table 1. User-Level Registers (continued)**

Register	Description
Condition code register (CCR)	The CCR is the lower byte of the SR. It contains indicator flags that reflect the result of a previous operation and are used for conditional instruction execution.
MAC status register (MACSR)	Defines the operating configuration of the MAC unit and contains indicator flags from the results of MAC instructions.
Accumulator (ACC)	General-purpose register used to accumulate the results of MAC operations
Mask register (MASK)	General-purpose register provides an optional address mask for MAC instructions that fetch operands from memory. It is useful in the implementation of circular queues in operand memory.

### 1.4.3 Supervisor Registers

Table 2 summarizes the MCF5307 supervisor-level registers.

**Table 2. Supervisor-Level Registers**

Register	Description
Status register (SR)	The upper byte of the SR provides interrupt information in addition to a variety of mode indicators signaling the operating state of the ColdFire processor. The lower byte of the SR is the CCR, as shown in Figure 4.
Vector base register (VBR)	Defines the upper 12 bits of the base address of the exception vector table used during exception processing. The low-order 20 bits are forced to zero, locating the vector table on 0-modulo-1 Mbyte address.
Cache configuration register (CACR)	Defines the operating modes of the Version 4 cache memories. Control fields configuring the instruction, data, and branch cache are provided by this register, along with the default attributes for the 4-Gbyte address space.
Access control registers (ACR0/1)	Define address ranges and attributes associated with various memory regions within the 4-Gbyte address space. Each ACR defines the location of a given memory region and assigns attributes such as write-protection and cache mode (copyback, write-through, cacheability). Additionally, CACR fields assign default attributes to the instruction and data memory spaces.
RAM base address register (RAMBAR)	Provide the logical base address for the 4-Kbyte SRAM module and define attributes and access types allowed for the SRAM.
Module base address register (MBAR)	Defines the logical base address for the memory-mapped space containing the control registers for the on-chip peripherals.

### 1.4.4 Instruction Set

The ColdFire instruction set supports high-level languages and is optimized for those instructions most commonly generated by compilers in embedded applications. Section 2.6, “Instruction Set Summary,” in the *MCF5307 User’s Manual* provides an alphabetized listing of the ColdFire instruction set opcodes, supported operation sizes, and assembler syntax. For two-operand instructions, the first operand is generally the source operand and the second is the destination.

Because the ColdFire architecture provides an upgrade path for 68K customers, its instruction set supports most of the common 68K opcodes. A majority of the instructions are binary compatible or optimized 68K opcodes. This feature, when coupled with the code conversion tools from third-party developers, generally minimizes software porting issues for customers with 68K applications.





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